CLAIMS

1. A controlled voltage swing data bus circuit for transferring data to a data bus, comprising:
   a. a pass transistor coupled with the bus;
   b. a discharge transistor coupled with the pass transistor and ground, ~~the discharge transistor programmed to impose a first preselected bus operational characteristic on the data bus~~; and
   c. an inverter coupled between the discharge transistor and the pass transistor, the inverter and the discharge transistor forming a signal node, the inverter selectably driving the pass transistor gate, responsive to a signal node voltage value.

2. The controlled voltage swing data bus circuit of Claim 1, wherein the pass transistor is programmed to impose a second preselected bus operational characteristic on the data bus.

3. The controlled voltage swing data bus circuit of Claim 1, further comprising a plurality of discharge transistors, ones of the plurality of discharge transistors being selectively programmed to impose respective preselected bus operational characteristics on the data bus.

4. The controlled voltage swing data bus circuit of Claim 1, wherein the pass transistor couples the data bus with one of a global sense amplifier, a local sense amplifier, a global wordline decoder, and a local wordline decoder.

5. The controlled voltage swing data bus circuit of Claim 2, wherein the pass transistor couples the data bus with one of a global sense amplifier, a local sense amplifier, a global wordline decoder, and a local wordline decoder.

6. A controlled voltage swing data bus transfer circuit for transferring data between a first data bus and a second data bus, comprising:

a. a first inverter;

b. a first pass transistor, coupled between the first data bus and the first inverter, the coupling of the first pass transistor and the first inverter forming a first signal node;

c. a second inverter ~~cross-linked to the first inverter~~;

d. a second pass transistor, coupled between the second data bus and the second inverter, the coupling of the second pass transistor and the second inverter forming a second signal node;

e. a first signal discharge transistor coupled between the first signal node and ground; and

f. a second signal discharge transistor coupled between the second signal node and ground, wherein the first inverter transfers a signal representative of first data on the first data bus to the second signal discharge transistor and the second inverter transfers a signal representative of second data on the second data bus to the first signal discharge transistor.

7. The controlled voltage swing data bus transfer circuit of Claim 6, further comprising:

a. a first node charge transistor, coupled between V_{dd} and the first signal node;

b. a first node discharge transistor coupled between the first signal discharge transistor and ground;

c. a second charge transistor, coupled between V_{dd} and the second signal node;

d. a second node discharge transistor coupled between the second signal discharge transistor and ground, wherein each of the first and second node charge

transistors pull the respective first and second signal node to V_{dd}, when a LOW gate signal is applied thereto.

8. The controlled voltage swing data bus transfer circuit of Claim 7, further comprising a clocking signal operably coupled with the first node charge transistor, the first node discharge transistor, the second node charge transistor, and the second node discharge transistor.

9. The controlled voltage swing data bus transfer circuit of Claim 6, wherein one of the first data bus and the second data bus is coupled with one of a global sense amplifier, a local sense amplifier, a global wordline decoder, and a local wordline decoder.

10. The controlled voltage swing data bus transfer circuit of Claim 8, wherein one of the first data bus and the second data bus is coupled with one of a global sense amplifier, a local sense amplifier, a global wordline decoder, and a local wordline decoder.